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Ultra Low Power Design and High Speed Design of Domino Logic Circuit

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Abstract
The tremendous success of the low-power designs of VLSI circuits over the past 50 years has significant change in our life style. Integrated circuits are everywhere from computers to automobiles, from cell phones to home appliances. Domino logic is a CMOS based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. Dynamic logic circuits are used for their high performance, but their high noise and extensive leakage has caused some problems for these circuits. Dynamic CMOS circuits are inherently less resistant to noise than static CMOS circuits. In this paper we proposed different domino logic styles which increases performance compared to existing domino logic styles. According to the simulations in cadence virtuoso 65nm CMOS process, the proposed circuit shows the improvement of up thirty percent compared existing domino logics.
Keywords:- Domino Logic, Dynamic Node, Evaluation Network, Low power Consumption.

I. Introduction

The tremendous success of the low-power designs of VLSI circuits over the past 50 years has significant change in our life style. Integrated circuits are everywhere from computers to automobiles, from cell phones to home appliances. The growth of the low-power circuits is predicted to continue at faster pace. Since the first integrated circuit was invented in the labs of Texas instruments in 1958. The integrated capacity of the transistors on a single chip is doubling every two to three years [1]. In 1965, Gorden Moore showed that for any MOS transistor technology there exists a minimum cost that maximizes the number of components per integrated circuit. He also predicted that as transistor dimensions are shrunk from onetechnology generation to the next, the minimal cost point allows doubling the number of transistor every two to three years. This trend has been sustained and is expected to be maintained well into first 20 years of this century. With the dramatic increase in chip complexity ULSI (Ultra Large Scale Integration), number of transistors and power consumption are growing rapidly. The objective of designing digital VLSI circuits is to minimize silicon area per logic circuit as to have large number of gates per chip. Area reduction occurs in three different ways: (i) advances in processing technology that enable reduction of the minimum device size (ii) circuit design techniques (iii) careful chip layout. Power consumption and signal delay are crucial elements in designing of high-performance low voltage VLSI circuits. The reduction of power dissipation and the improvement of the speed require optimization at all levels in the design procedure. In nano-scaling, enormous power is consumed as static power dissipation[2].

The domino circuits are used in various circuits, especially-memory [3-5], multiplexor,comparator [6], and arithmetic circuit. [7-8] and also used in full adders that are most important part of a CPU. Additionally, domino circuits are important components in other applications such as digital signal processing (DSP) architectures and microprocessors [9], which rely on the efficient implementation of generic arithmetic logic and floating point units to execute dedicated algorithms. Various design approaches had been investigated for realizing domino CMOS topologies in the literature [10]. The Extensive use of high speed domino circuits attracts many researchers in this field. There are various issues related to domino circuits, such as power consumption, speed and noise immunity [11.

II. Literature Review

Domino logic is a CMOS logic style obtained by adding a static inverter to the output of the basic dynamic gate circuit, it can be used to implement non-inverting functions [3, 12]. The resulting structure is shown in Fig.1.6. Domino CMOS circuit has advantage in terms of high speed and wide fan-in over static CMOS circuits.The domino CMOS circuit suffers from noise margin problem due to charge redistribution between parasitic capacitances at the internal nodes of the circuit and hence false output may be resulted. Domino logic consists of a single clock, which is used to precharge the dynamic node of the circuit in precharge phase and to evaluate the

function made by NMOS network in evaluation phase.

Designs of digital integrated circuits rely on three major criteria: Low power consumption, small chip area and high speed. In VLSI design, the selection of logic family is dictated by the system performance as shown in Fig.1. Table.1. summarizes the performance comparisons of logic styles [13]. From the table domino CMOS circuit has higher speed and it require lower area as compared to other logic style. High speed operation of domino circuits is primarily due to the lower noise margins of domino circuits as compared to static gates.

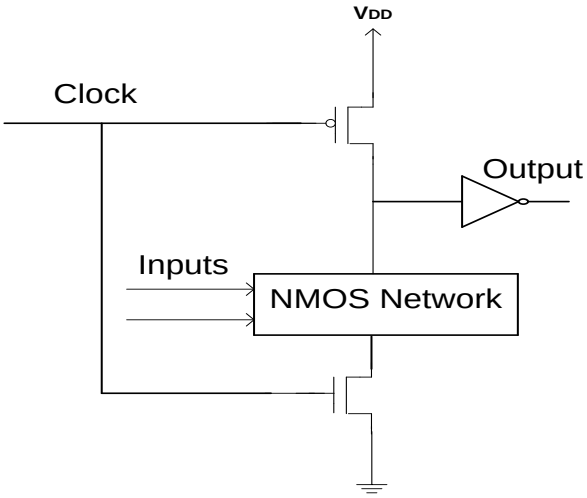

Fig. 1. A domino CMOS circuit.

Table I. summarizes the performance comparisons of logic styles [13].

Logic Families	**Speed**	**Power Consumption**	**Noise Margin**	**Area**
Static CMOS	Medium	Medium	High	High
Pseudo NMOS	Fast	High	Medium	Low
Dynamic CMOS	Fast	High	Low	Low
Domino CMOS	Fast	High	Low	Low

(a) Footless Standard Domino Logic & Footed Standard Domino Logic

Firstly considering the footless standard domino logic and footed standard domino logic as shown in Fig.2 and 3. In conventional domino logic, a keeper transistor is utilized as a feedback for retaining the state of the dynamic node. But the resulting contention between the keeper transistor and pull down networks reduces the power and speed characteristics of the circuit [14]. Now in comparison with the footless standard domino logic, footed standard domino logic achieves better immunity to noise due to the stacking effect. To achieve the improvement in robustness of the standard domino circuits, keeper upsizing can be done. But this upsizing of keeper transistor results in contention which degrades the power and evaluation delay characteristics of the conventional domino circuits [15].

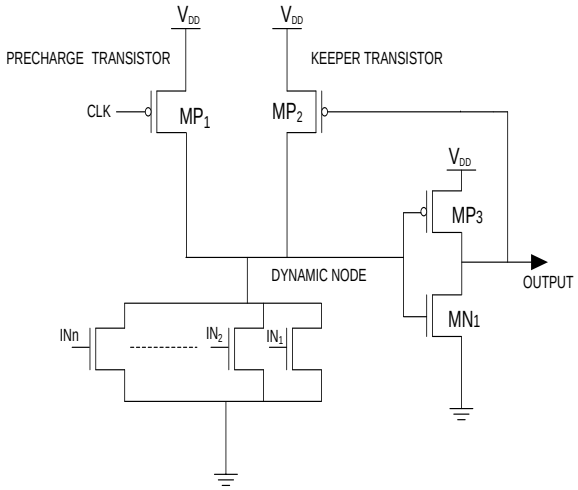

Fig.2 Standard Footerless Domino Logic Circuit

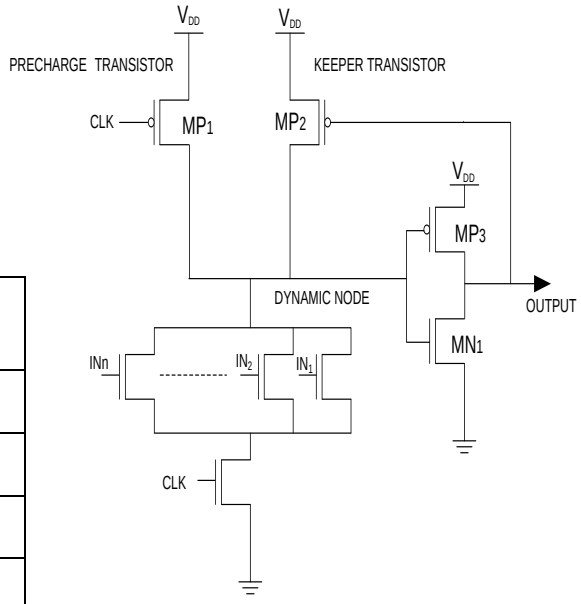

Fig.3 Standard Footed Domino logic circuit

(b) Conditional Keeper Domino Logic

Now considering the another efficient technique that is Conditional Keeper Domino Logic (CKDL) which is shown in Fig.4. that make use of two keeper transistors [9]. One of the two keeper transistors is weaker one (K1) and other one is stronger (K2) as shown in Fig.2. In the working, initially K1 is on during the starting of evaluation phase for maintaining the state of dynamic node. If the state of dynamic node being retained high after the delay for inverters, then that will make the stronger keeper K2 to be turned on. This method results in the reduction

of contention and also improves noise immunity. Noise characteristics can further be reduced by the sizing of delay elements but this will give rise to the higher power dissipation. And area overhead is also one disadvantage due to NAND gate for CKDL [16].

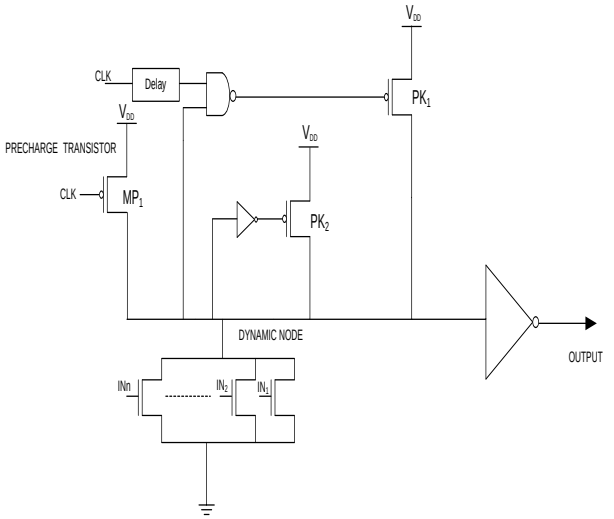

Fig. 4 Conditional Keeper Domino Logic

(c) High Speed Domino Logic

High speed domino logic is another configuration shown in figure 3. The working of this domino logic results in the reduction of the contention between the keeper transistor and the evaluation network with a use of clock delay as shown in Fig.5. As comparison to the CKDL technique it makes use of only strong keeper and eliminates the weaker one so as to enhancing speed. This keeper transistor remains off at the starting of the evaluation phase which results in the current reduction, but at the cost of power consumption, area overhead and lower noise immunity due to the float dynamic node [10].

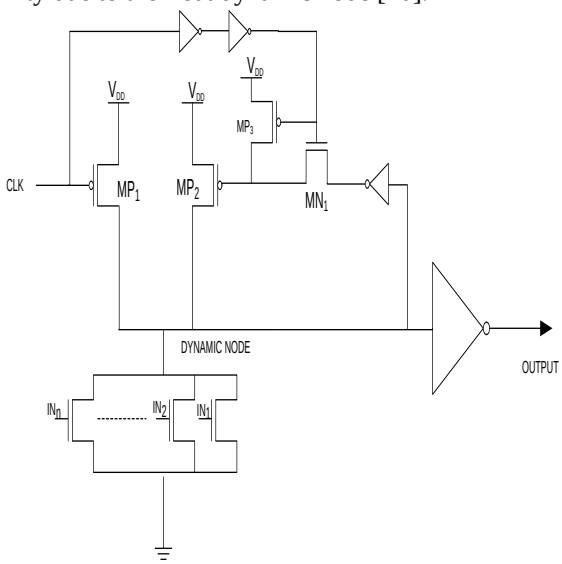

Fig.5 High-Speed Domino Logic

(d) Diode Footed Domino Logic

Diode footed domino logic is another technique presented in [17]. Customization to the standard domino circuit has been done by adding NMOS transistor in a diode configuration in series with the evaluation network as shown in Fig.6. This diode footer (M1) results in the sub threshold leakage reduction due to the stacking effect [12,18-20]. But there is performance degradation due to the diode footer that's why mirror transistor [M2] is employed to increase the performance characteristic.

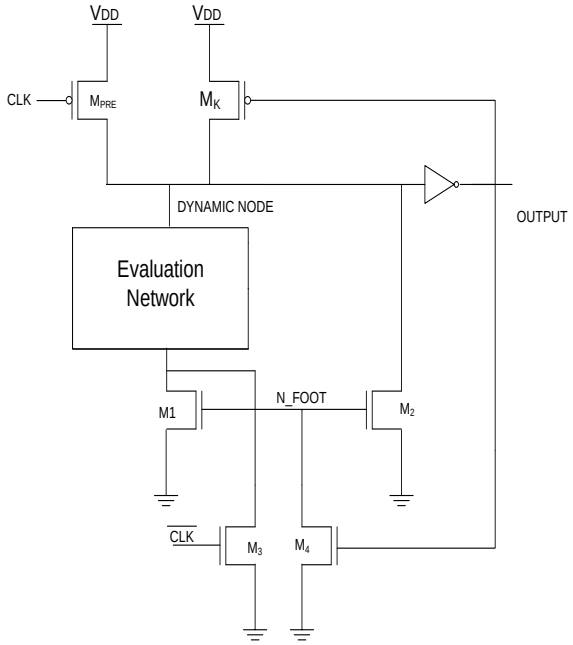

Fig.6. Diode Footed Domino Logic

Current-Comparison Domino

The proposed technique uses the difference and the comparison between the leakage current of the OFF Transistors and the switching current of the ON transistors of the pull down network to control the PMOS keeper transistor,yielding reduction of the contention between keeper transistor and the pull down network from which previously proposed techniques have suffered. Moreover, using the stacking effect, leakage current is reduced and the performance of the current mirror is improved.

In this circuit, the reference current is compared with the pull down network current. If there is no conducting path from the dynamic node to the ground and the only current in the PDN is the leakage current, the keeper transistor will not turn off because the reference current is greater than the leakage current. In fact there is a race between the pull down network and the reference current.The current, which is greater than the other wins the race and turns off its keeper PMOS transistor. Transistor M_{pre2} is removed to discharge node K and thus turning on the keeper transistor in the precharge phase. This results in improved noise immunity. There- fore, unlike circuit designs such as HSdomino in which the keeper

transistor is off at the beginning of the evaluation phase,the keeper transistor is on in this design.

The proposed domino circuit is shown in Fig. 7. In this circuit M_1 is added in series with the evaluation network such as the wide OR gate, as illustrated in this schematic.

The two phases of the proposed circuit in active mode are explained as follows:

In the precharge phase, clock voltage is in low level (CLK='0' in Fig. 7). Hence, transistors M_{pre}, M_{keeper} and M_8 are on and M_1 and M_2 are off. Therefore, the voltage of the dynamic node (Dyn_n) is raised to the high level by transistor M_{pre}.In this phase, the leakage current is decreased due to the stacking effect since the minimum voltage of a MOS transistor in diode configuration is equal to $V_{gs}=V_{ds}=V_{tn}$, where V_{tn} is the NMOS threshold voltage.

In the evaluation phase, clock voltage is in the high level (CLK='1' in Fig.7), so the transistors such as M_{pre} and M_8 are turned off. Depending on inputs levels, the other transistors may be turned on. According to the discharging current of PDN and the mirror current, two states may occur. The gate voltage of the keeper transistor depends upon which current is greater than the other. Then due to the positive feedback consisting of M_4 and M_{keeper} , the voltage of node K is determined.

First, if all inputs are in low level, the mirror current is greater than the PDN leakage current, the voltage of node K is discharged to zero. Therefore, the keeper transistor is turned on and maintains the dynamic node at a high level.

Second, if at least one input is at a high level, the discharging current of PDN is higher than the mirror current,yielding the voltage of node K to remain high.This reduces the contention problem by turning off the keeper transistor with any great change in the current of the NMOS pull down network rather than the mirror current.

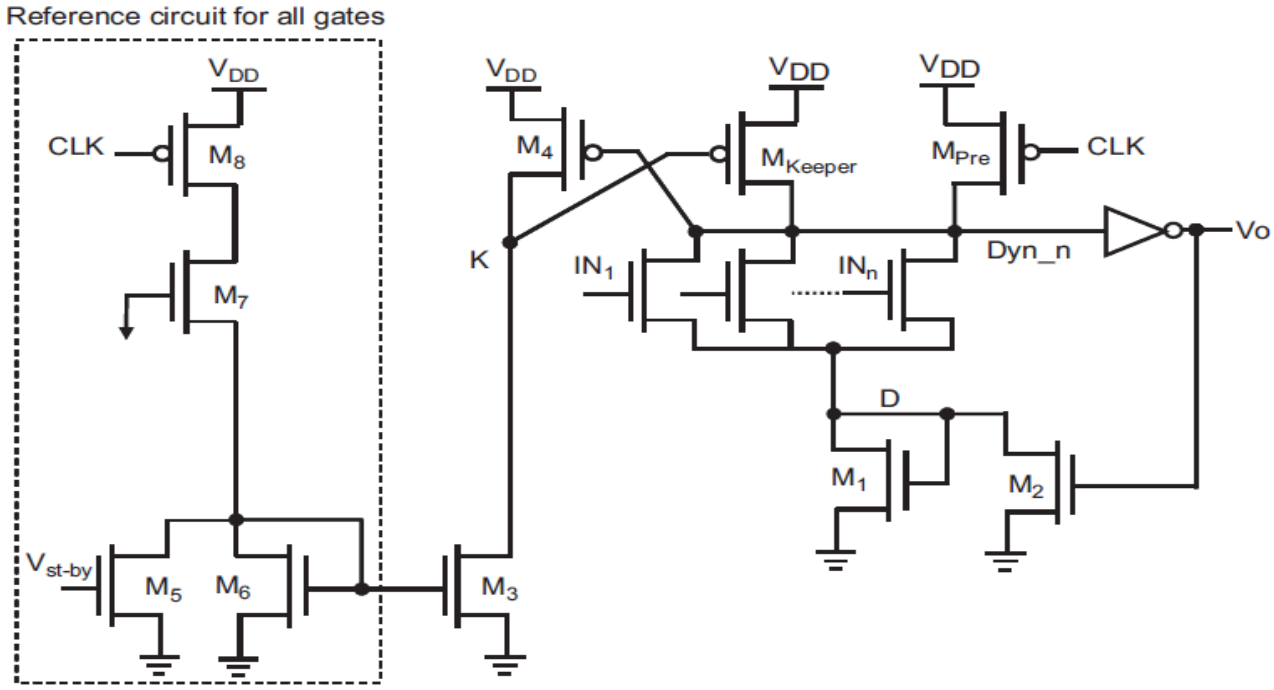

Fig. 7. An n-Input Current Comparison Domino OR gate

III. Proposed Circuit

We can get the fully domino logics in two ways.

1) Just by excluding clock input PMOS
2) Or just by replacing the clock signal with an Enble signal

In the first circuit we are excluding clock input PMOS transistor and we are using a weak PMOS instead of clock driver. Weak device charging rate is very slow, so when there is no input applied for a long time this transistor makes dynamic node to charge upto supply voltage level. So there will be no contention problem with this circuit. So we do not need any separate path to discharge at the beginning of evaluation phase. We can exclude the delayed version of clock. The modified domino circuit for full static operation shown in Fig.8.

The above circuit consists of an extra enable signal, which should be enabled always to get static output even in precharge phase. The circuit operation is as follows: when the clock is low (normally said as precharge phase), the transistor MN1 is in OFF condition. According to the input logics dynamic node may charged to V_{DD} or discharged to GND.

If inputs makes dynamic node to discharge to footer voltage, then this potential makes use of level restorer to discharge as mentioned in previous

sections. And also can provide the exact outputs irrespective of clock. We used an external enable signal here, so GND level is brought upto the keeper circuit if no inputs makes to discharge the dynamic node and more than one transitions are allowed in every case.

But in the previous circuit, we can observe that the clock property is not used properly, and we avoided using clock operations to get our desired output i.e use of clock is surpassed here. And the cicuit is also working accurately, if we replaced the clock with an enable signal. It may not be said as a dynamic circuit as we are not using clock here, but we are using charge keeper circuit and static inverter, so it can be said as a domino circuit.

And in the second circuit, earlier we developed a static evaluation domino circuit which could able to allow more than one transitions in evaluation phase. So I am using extended evauation phase signal to get the fully static output.

The proposed circuit has additional evaluation transistor MN6 with gate connected to the CLK. When MN1 has voltage drop due to presence of noise-signals, MN2 starts leaking which causes a lot of power dissipation. This makes the circuit less noise robust. In proposed scheme, the transistor MN6 causes the stacking effect which makes gate-to-source voltage VGS of MN2, smaller (MN1 less conducting). Hence circuit becomes more noise robust and less leakage power consuming.

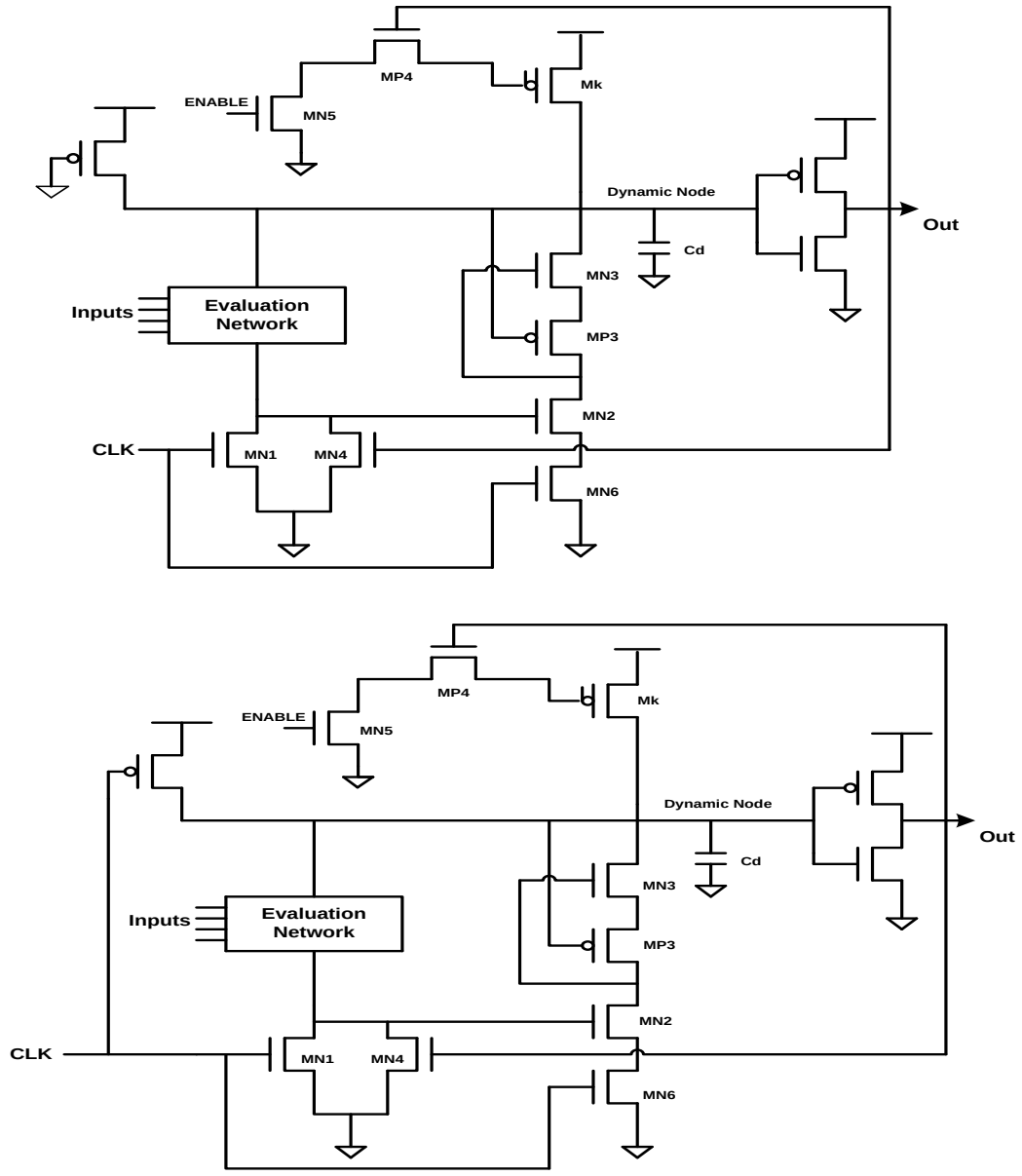

Fig.8. Proposed Circuit

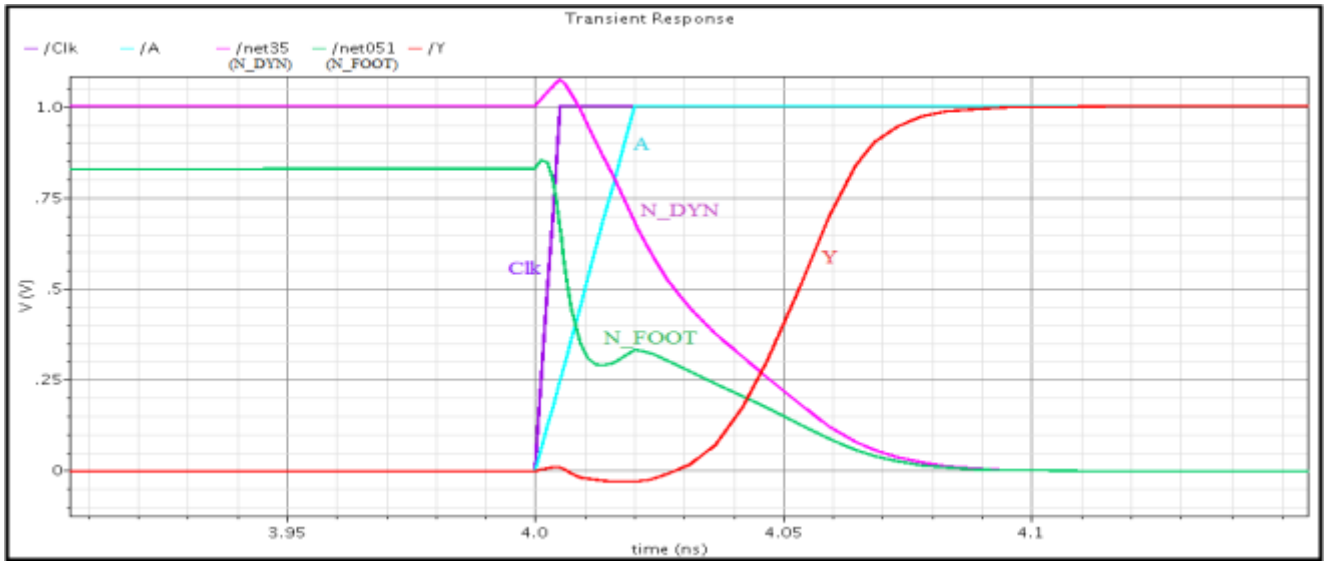

Fig.9.Simulated waveform of proposed scheme

IV. Results and Dissuasion

Simulations are performed in 90nm and 65 nm technology at 100MHz frequency and V_{DD} of 1V and 0.9V. The fall/rise times of the waveforms were set to 1pS. Considering the application of wide OR gates delay, power dissipation and UNG (Unit Noise Gain) has been calculated for 8 input and 16 input OR gate to compare different topologies. Fig.9 provides proper logic of footed domino logic circuit. For calculation of UNG [11], a pulse noise is applied to all inputs with amplitude which is a fraction of supply voltage and a pulse width equal to 30% of duty cycle. Then, the amplitude of the input noise pulse is increased until the amplitude of the resulting output noise voltage is equal to that of the input noise signal. This noise amplitude is defined as

UNG= Vin,Vnoise = Voutput

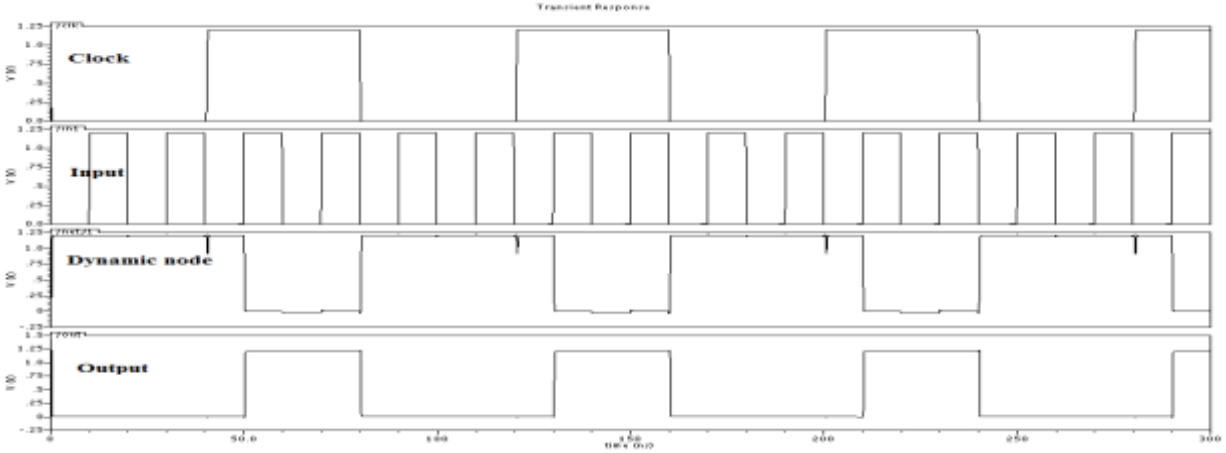

Fig. 9. Output waveform of Footed Domino Logic

Table.II. Simulation is done with V_{dd}=1v, Frequency is 100MHz, For 8 Input OR Gate at 90nm Process Technology

Parameters	FLD	FD	HSD	CKD	DFD	LCR	CCD	Proposed Circuit
Power (µW)	2.203	2.964	375.49	205.52	3.320	2.259	1.98	2.104
Normalized power	1	1.34	170.4	93.29	1.50	1.025	0.9	0.955
Propagation delay (ps)	16.55	29.615	16.152	19.05	27.88	16.91	18.13	17.25
Normalized propagation delay	1	1.78	0.97	1.15	1.68	1.02	1.09	1.04
Power delay product (aJ)	36.45	87.64	6064.1	3915.1	92.56	38.19	35.89	36.29
UNG	0.398	0.427	0.3962	0.4079	0.429	0.4441	0.493	0.510
Normalized UNG	1	1.072	0.995	1.024	1.077	1.115	1.23	1.28
No. of Transistors	12	13	18	23	16	14	23	20

Table.III. Simulation is done with V_{dd}=0.9v, Frequency is 100MHz, For 8 Input OR Gate at 65nm Process Technology

Parameters	FLD	FD	HSD	CKD	DFD	LCR	CCD	Propsed Circuit
Power (µW)	1.809	2.201	276.53	137.32	2.647	1.882	1.648	1.701
Normalized power	1	1.21	152.86	75.90	1.46	1.04	0.911	0.940
Propagation delay (ps)	14.96	25.46	14.655	16.81	24.83	15.05	16.65	15.35
Normalized propagation delay	1	1.70	0.979	1.12	1.65	1.06	1.11	1.026
Power delay product (aJ)	27.06	56.03	4044.7	2303.9	65.72	28.32	27.43	26.11
UNG	0.298	0.327	0.3062	0.3179	0.331	0.310	0.361	0.381
Normalized UNG	1	1.097	1.027	1.066	1.110	1.040	1.211	1.27
No. of transistors	12	13	18	23	16	14	23	28

IV. Conclusion

A new structure of domino logics has been proposed which gives the exact output as static gates with use of a regular clock signal. Proposed fully static domino logics has lowest PDP as well as robust capability at 1V supply voltage. Proposed domino logics in section III is a fully static domino gate, which can provide exact output even in precharge phase. It has been observed that our proposed domino styles have optimum performance in terms of PDP and output voltage swing. However, proposed domino logic circuits are not free from glitch noise power dissipation. It is observed when we used a high frequency inputs. Also our proposed domino circuits have more number of transistors and , our proposed multipliers suffer from complex design. Finally, it has been examined that the proposed circuits have optimum performance in terms of power dissipation, delay and output reliability. All simulation are done using CADENCE UMC 65nm environment.

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